AMENDMENT TO THE CLAIMS

1. (Previously Amended) A method for forming a raised source/drain contact structure for a semiconductor transistor, comprising the steps of:

providing a transistor gate on a substrate surface, and a source/drain region defined as a surface region extending laterally from said transistor gate to an isolation structure formed one of on said substrate and in said substrate;

forming a doped amorphous silicon layer over and contacting said source/drain region and over said isolation structure, said doped amorphous silicon layer including dopant impurities therein;

converting said amorphous silicon layer to a crystalline silicon layer using selective laser annealing, said converting urging at least some of said dopant impurities to diffuse into said source/drain region; and

patterning said crystalline silicon layer to form a raised source/drain contact structure covering said source/drain region and extending over at least part of said isolation structure.

2. (Original) The method as in claim 1, in which said amorphous silicon layer includes dopant impurities therein prior to said step of converting, and said step of converting urges at least some of said dopant impurities to diffuse into said source/drain region.

3. (Original) The method as in claim 1, further comprising the step of forming an insulating layer over said raised source/drain contact structure and forming at least one contact opening through said insulating layer to expose a corresponding portion of said raised source/drain contact structure, each portion including sections of said corresponding raised source/drain contact structure formed over said corresponding isolation structure.

4. (Original) The method as in claim 1, wherein the step of converting comprises converting said amorphous silicon layer to a polycrystalline silicon layer.

5. (Original) The method as in claim 1, wherein the step of converting comprises converting said amorphous silicon layer to a substantially single crystalline silicon layer.

6. (Original) The method as in claim 1, wherein said step of converting comprises using an excimer laser for said selective laser annealing.

7. (Original) The method as in claim 6, in which said step of converting includes an XeCl excimer laser emitting light having a wavelength of approximately 308 nanometers.

8. (Original) The method as in claim 6, wherein said excimer laser emits radiation at or near the absorption peak of silicon.

9. (Original) The method as in claim 8, in which said transistor gate comprises a metal gate and said step of converting does not melt said metal gate.

10. (Original) The method as in claim 1, in which said step of providing a transistor gate includes said transistor gate being covered by an insulating material.

11. (Original) The method as in claim 1, further comprising removing sections of said amorphous silicon layer thereby forming at least one discrete section of amorphous silicon, prior to said step of converting.

12. (Original) The method as in claim 1, further comprising implanting impurities into said crystalline silicon layer and said source/drain region after said step of converting.

13. (Newly Amended) A method for forming a raised source/drain contact structure for a semiconductor transistor, comprising the steps of:

providing a transistor gate on a substrate surface and a source/drain region, defined as a surface region extending laterally from said transistor gate to an isolation structure formed one of on said substrate and in said substrate;

forming a doped amorphous silicon layer over and contacting said source/drain region and said isolation structure, said doped amorphous silicon layer including dopant impurities therein;

patterning said amorphous silicon layer to form a raised source/drain contact structure covering said source/drain region and extending over at least part of said isolation structure; and

converting said amorphous silicon raised source/drain contact structure to a crystalline silicon raised source/drain contact structure by selectively laser annealing the structure, said converting urging at least some of said dopant impurities to diffuse into said source/drain region.

14. (Original) The method as in claim 13, in which said amorphous silicon layer includes dopant impurities therein prior to said step of converting, and said step of converting urges at least some of said dopant impurities to diffuse into said source/drain region.

15. (Original) The method as in claim 13, wherein said step of converting comprises using an excimer laser for said selective laser annealing.

16. (Original) The method as in claim 15, wherein said excimer laser emits radiation at or near the absorption peak of silicon.

17. (Previously Amended) A method for forming a raised source/drain contact structure for a semiconductor transistor, comprising the steps of:

providing a transistor gate on a substrate surface, and opposed source/drain regions, each source/drain region defined as the surface region

extending laterally from said gate to a corresponding isolation structure formed one of on said substrate and in said substrate;

forming a doped amorphous silicon layer over and contacting each said source/drain region and over each said corresponding isolation structure, said doped amorphous silicon layer including dopant impurities therein;

converting said amorphous silicon layer to a crystalline silicon layer using selective laser annealing, said converting urging at least some of said dopant impurities to diffuse into said source/drain regions; and

patterning said crystalline silicon layer to form a duality of raised source/drain contact structures, each covering said corresponding source/drain region and extending over at least part of said corresponding isolation structure.

18. (Original) The method as in claim 17, in which said amorphous silicon layer includes dopant impurities therein prior to said step of converting, and said step of converting urges at least some of said dopant impurities to diffuse into said source/drain regions.

19. (Original) The method as in claim 17, wherein said step of converting comprises using an excimer laser for said selective laser annealing.

20. (Previously Amended) A method for forming a semiconductor structure, comprising the steps of:

providing an exposed surface of a semiconductor substrate, said exposed surface bounded laterally by at least one isolation structure;

forming a discrete amorphous silicon layer contacting said exposed surface and extending laterally over at least portions of at least one of said at least one isolation structure, said discrete amorphous silicon layer including dopant impurities therein; and

selectively laser annealing said discrete amorphous silicon layer, thereby converting said discrete amorphous silicon layer to a discrete single crystalline silicon layer and driving at least some of said dopant impurities into said exposed surface.

21. (Original) The method as in claim 20, in which said discrete amorphous silicon layer includes dopant impurities incorporated therein, and step of converting urges at least some of said dopant impurities to diffuse into said exposed substrate surface.

22. (Original) The method as in claim 20, wherein said step of selectively laser annealing includes irradiating with light emitted by an excimer laser.

23. (Original) The method as in claim 20, in which said step of selectively laser annealing includes using an excimer laser which emits light at a wavelength at or near the absorption peak of silicon, and produces an energy fluence chosen to anneal substantially only said discrete amorphous silicon layer.

24. (Previously Amended) A method for forming a transistor comprising:

providing a semiconductor substrate having a surface;

providing a transistor region between isolation structures formed in said substrate;

forming a gate stack, including a gate electrode formed over a gate dielectric, in a central portion of said transistor region, said gate stack covered with an insulating material, the lateral portions of said transistor region not covered by said gate stack being designated source/drain regions;

forming a discrete amorphous silicon film over said transistor region, said discrete amorphous silicon film including dopant impurities therein;

irradiating with a laser beam, then allowing cooling, thereby converting said discrete amorphous silicon film to a crystalline silicon film and urging the diffusion of at least some of said dopant impurities into said source/drain regions; and

forming an opposed duality of discrete raised source/drain contact structures from said crystalline silicon film, by removing portions of said crystalline silicon film, each raised source/drain contact structure formed over a corresponding source/drain region.

25. (Original) The method as in claim 24, in which said step of forming said discrete amorphous silicon film includes forming said discrete amorphous silicon film over said transistor region and further extending over said isolation structures and in which said step of forming discrete raised source/drain contact structures includes each raised source/drain contact structure extending over said corresponding isolation structure.

26. (Previously Amended) The method as in claim 24, further comprising forming a dielectric structure over said surface prior to the step of forming said discrete amorphous silicon film, portions of said dielectric structure encroaching said transistor region and in which said step of forming a discrete amorphous silicon film includes forming said discrete amorphous silicon film over at least portions of said dielectric structure.

27. (Previously Added) A method for forming a raised source/drain contact structure for a semiconductor transistor, comprising the steps of:

providing a metal transistor gate on a substrate surface, and a source/drain region defined as a surface region extending laterally from said metal transistor gate to an isolation structure, formed one of on said substrate and in said substrate;

forming an amorphous silicon layer over and contacting said source/drain region and over said isolation structure;

converting said amorphous silicon layer to a crystalline silicon layer using selective laser annealing without melting said metal transistor gate; and

patterning said crystalline silicon layer to form a raised source/drain contact structure covering said source/drain region and extending over at least part of said isolation structure.